depth, wherein the plurality of first semiconductor regions and the plurality of second semiconductor regions are formed and defined respectively;

wherein the body region is exposed between the plurality of second semiconductor regions and the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

2. (Previously Cancelled)

3. (Previously Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

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4. (Previously Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

5. (Original) A semiconductor device according to claim 1, further comprising a wiring member connected to at least one of the plurality of trench gates.

6. (Previously Cancelled)

7. (Original) A semiconductor device according to claim 3, further comprising a wiring member connected to at least one of the plurality of trench gates.

8. (Original) A semiconductor device according to claim 4, further comprising a wiring member connected to at least one of the plurality of trench gates.

9. (Original) A semiconductor device according to claim 1, further comprising a wiring member connected to the body region and to the second semiconductor region.

10. (Previously Cancelled)

11. (Original) A semiconductor device according to claim 3, further comprising a wiring member connected to the body region and to the second semiconductor region.

12. (Original) A semiconductor device according to claim 4, further comprising a wiring member connected to the body region and to the second semiconductor region.

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13. (Currently Amended) A process for producing a semiconductor device comprising:

forming a body region of a first conductivity type in a semiconductor substrate, the body region having a major surface opposite to a surface shared between the semiconductor substrate and the body region;

forming a plurality of trench gates extending through the body region;

forming a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from said major surface of the body region, at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via films bordering and insulating the trench gates;

forming a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from said major surface of the body region that is less than the first depth, wherein the plurality of first semiconductor regions and the plurality of second semiconductor regions are formed and defined respectively; and

connecting the plurality of first semiconductor regions spaced apart from one another by the second semiconductor regions;

wherein the body region is exposed between the plurality of second semiconductor regions.

14. (Previously Cancelled)

15. (Previously Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor

regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

16. (Previously Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-shaped configuration.

17. (Original) A process according to claim 13, further comprising:

forming a wiring member connected to at least one of the plurality of trench gates.

18. (Original) A process according to claim 13, further comprising:

forming a wiring member connected to the body region and to the second semiconductor region.

Please add the following new claims:

19. (New) A semiconductor device according to claim 1, further comprising a plurality of noncontiguous third semiconductor regions of the first conductivity type whose major extension is in a direction parallel to both the major surface of the body region and the trench gates.

20. (New) A process according to claim 13, further comprising forming a plurality of noncontiguous third semiconductor regions of the first conductivity type whose major extension is in a direction parallel to both the major surface of the body region and the trench gates.